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| Document No. | 853-0129 |
| ECN No. | 86487 |
| Date of Issue | November 11, 1986 |
| Status | Product Specification |
| Memory Products | |

82S147 / 82S147A

4K-bit TTL bipolar PROM

DESCRIPTION

The 82S147 and 82S147A are field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S147 and 82S147A include on-chip decoding and one Chip Enable input for ease of memory expansion, and feature 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S147 and 82S147A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

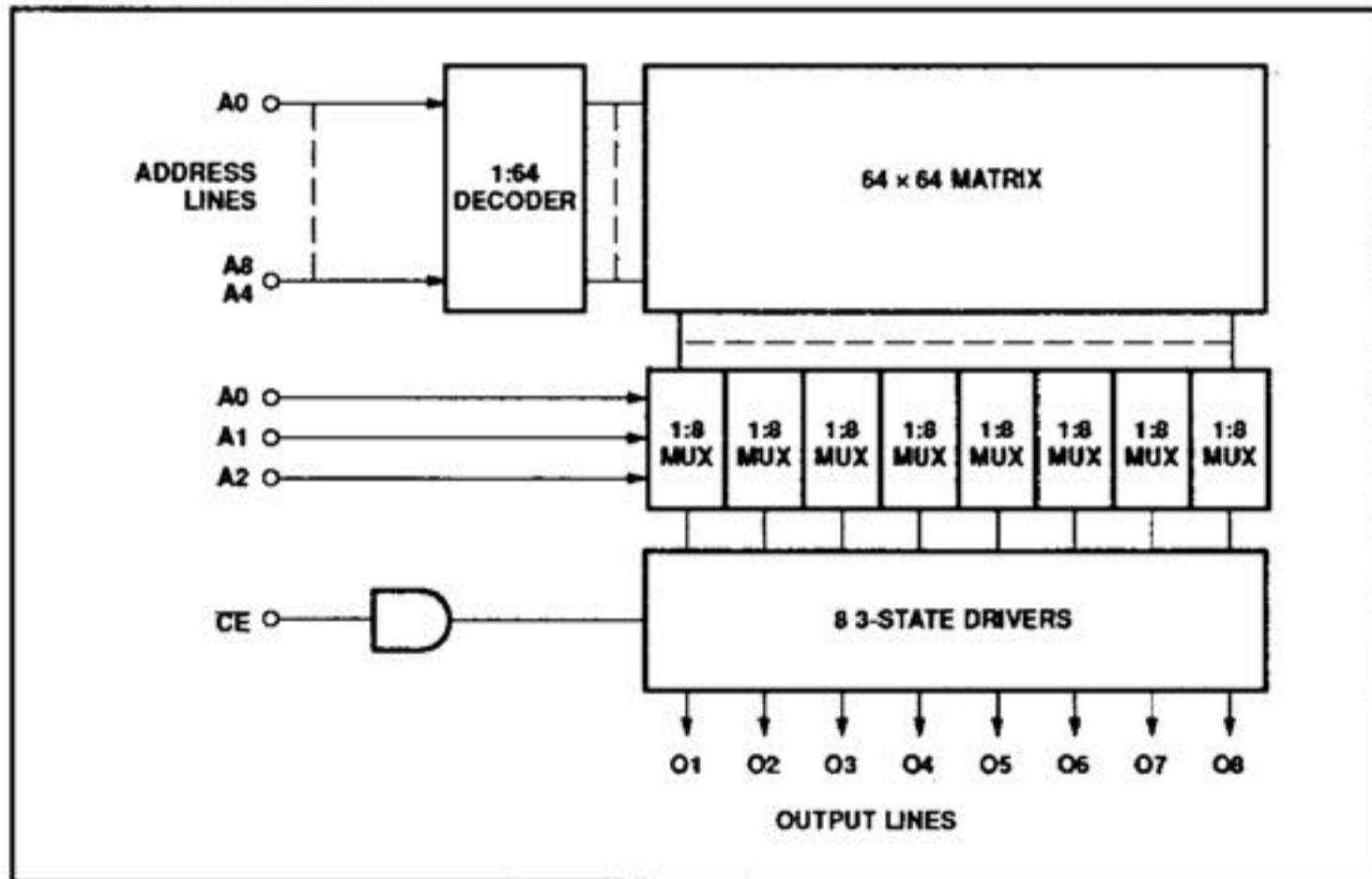
FEATURES

- Address access time:
 - N82S147: 60ns max
 - N82S147A: 45ns max
- Power dissipation: 625mW/bit typ
- Input loading: -100µA max
- One Chip Enable input
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Outputs: 3-State
- Unprogrammed outputs are Low level

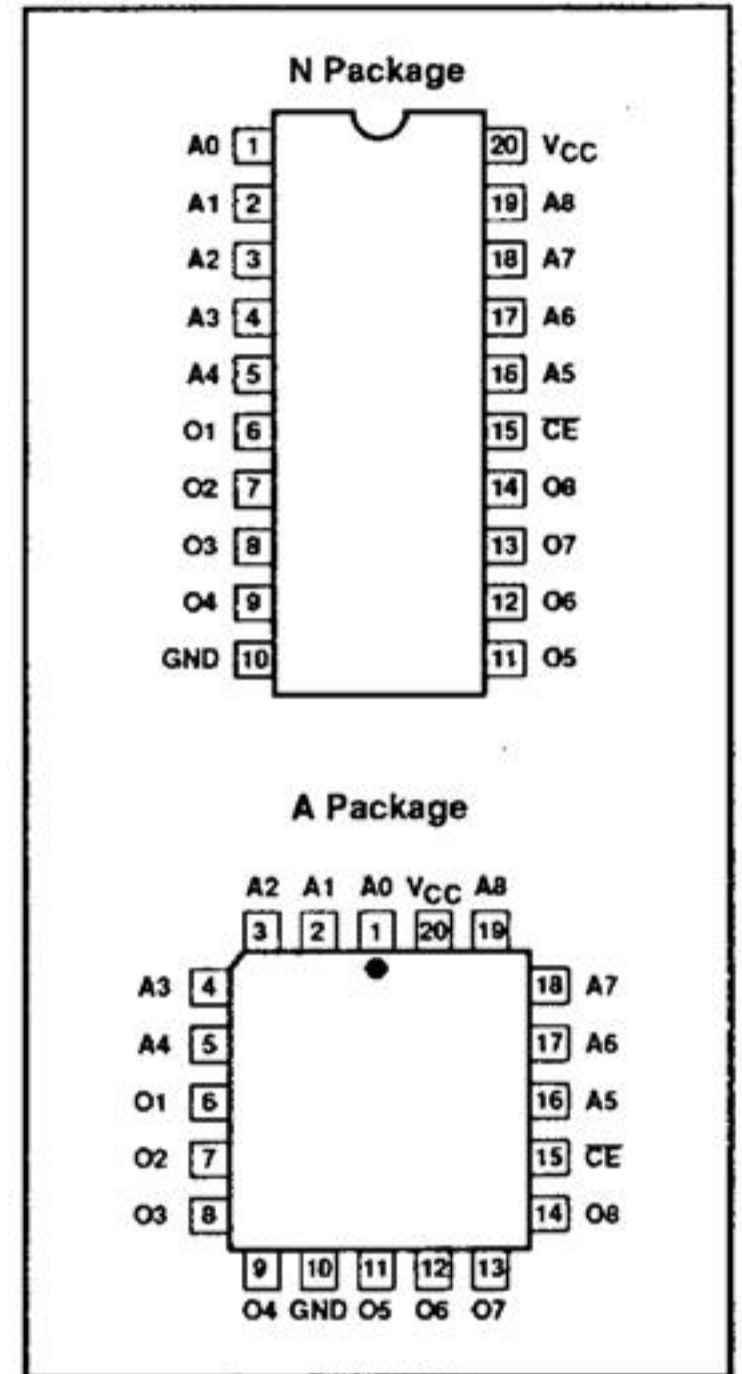
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

BLOCK DIAGRAM



PIN CONFIGURATIONS



4K-bit TTL bipolar PROM (512 × 8)**82S147 / 82S147A****ORDERING INFORMATION**

| DESCRIPTION | ORDER CODE |
|---|-----------------------|
| 20-Pin Plastic Dual-In-Line 300mil-wide | N82S147 N, N82S147A N |
| 20-Pin Plastic Leaded Chip Carrier 350mil-square | N82S147 A, N82S147A A |

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|-----------|-----------------------------|-------------|-------------|
| V_{CC} | Supply voltage | +7.0 | V_{DC} |
| V_{IN} | Input voltage | +5.5 | V_{DC} |
| V_O | Output voltage Off-State | +5.5 | V_{DC} |
| T_{amb} | Operating temperature range | 0 to +75 | $^{\circ}C$ |
| T_{stg} | Storage temperature range | -65 to +150 | $^{\circ}C$ |

DC ELECTRICAL CHARACTERISTICS $0^{\circ}C \leq T_{amb} \leq +75^{\circ}C$, $4.75V \leq V_{CC} \leq 5.25V$

| SYMBOL | PARAMETER | TEST CONDITIONS ^{1,2} | LIMITS | | | UNIT |
|-----------------------------------|----------------------------|--|--------|------------------|------|---------|
| | | | Min | Typ ³ | Max | |
| Input voltage | | | | | | |
| V_{IL} | Low | $I_{IN} = -12mA$ | 2.0 | | 0.8 | V |
| V_{IH} | High | | | | | |
| V_{IC} | Clamp | | | | | |
| Output voltage | | | | | | |
| V_{OL} | Low | $\overline{CE} = \text{Low}$ $I_{OUT} = 9.6mA$ | 2.4 | | 0.45 | V |
| V_{OH} | High | $I_{OUT} = -2mA$ | | | | |
| Input current | | | | | | |
| I_{IL} | Low | $V_{IN} = 0.45V$ | | | -100 | μA |
| I_{IH} | High | $V_{IN} = 5.5V$ | | | | |
| Output current | | | | | | |
| I_{OZ} | Hi-Z state | $\overline{CE} = \text{High}, V_{OUT} = 5.5V$ $\overline{CE} = \text{High}, V_{OUT} = 0.5V$ | -15 | | 40 | μA |
| I_{OS} | Short circuit ⁴ | $\overline{CE} = \text{Low}, V_{OUT} = 0V$ | | | | |
| Supply current⁵ | | | | | | |
| I_{CC} | | $V_{CC} = 5.25V$ | | 125 | 155 | mA |
| Capacitance | | | | | | |
| C_{IN} | Input | $\overline{CE} = \text{High}, V_{CC} = 5.0V$ $V_{IN} = 2.0V$ | | 5 | | pF |
| C_{OUT} | Output | $V_{OUT} = 2.0V$ | | 8 | | pF |

NOTES:

- All voltages with respect to network ground.
- Positive current is defined as into the terminal referenced.
- Typical values are at $V_{CC} = 5V$, $T_{amb} = +25^{\circ}C$.
- Duration of the short circuit should not exceed 1 second.
- Measured with all inputs grounded and all outputs open.

4K-bit TTL bipolar PROM (512 × 8)

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AC ELECTRICAL CHARACTERISTICS

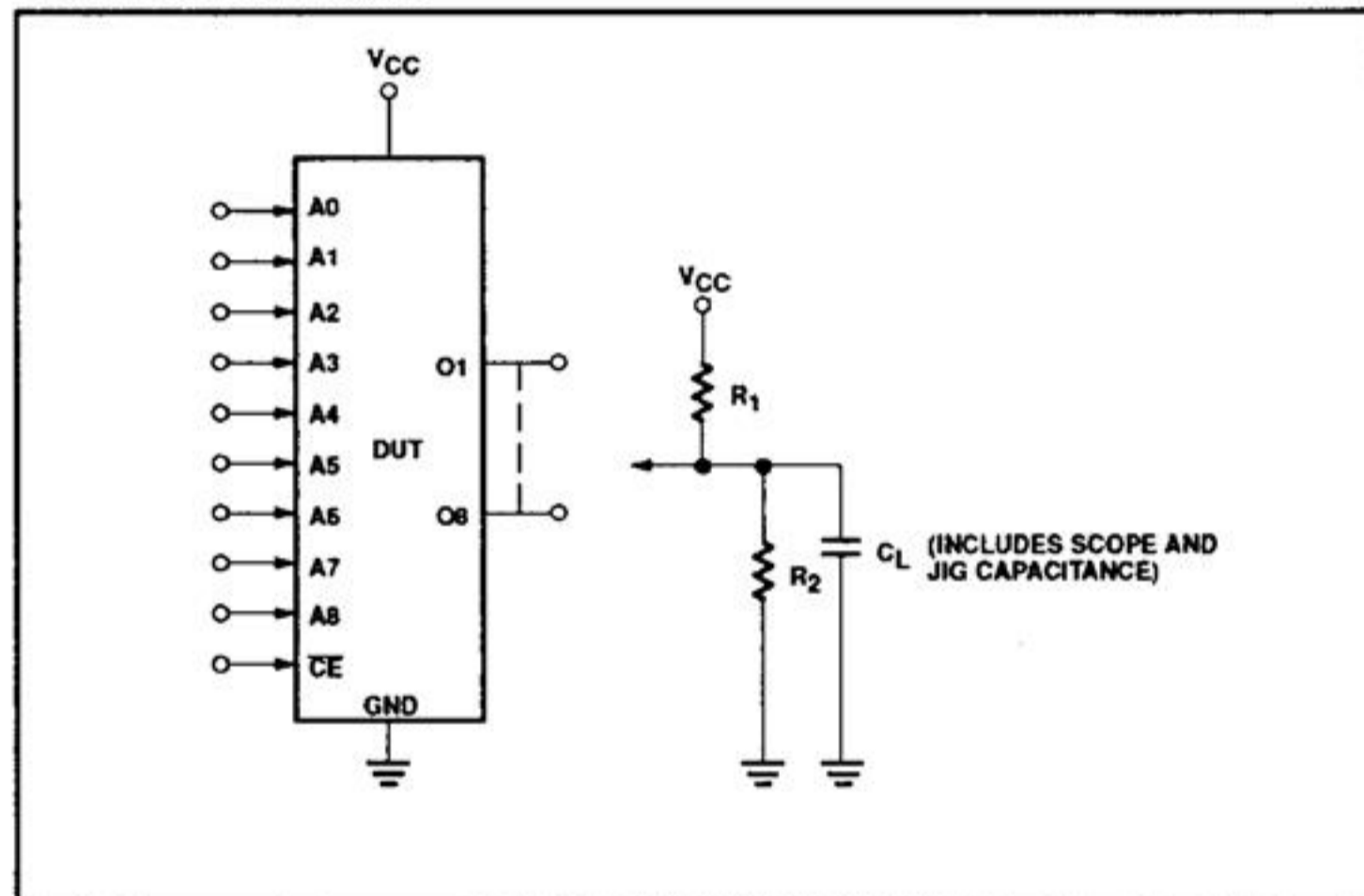
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

| SYMBOL | PARAMETER | TO | FROM | N82S147 | | | N82S147A | | | UNIT |
|---------------------------------|-----------|--------|--------------|---------|------------------|-----|----------|------------------|-----|------|
| | | | | Min | Typ ¹ | Max | Min | Typ ¹ | Max | |
| Access time² | | | | | | | | | | |
| t_{AA} | | Output | Address | | 45 | 60 | | 40 | 45 | ns |
| t_{CE} | | Output | Chip Enable | | 20 | 35 | | 20 | 30 | ns |
| Disable time³ | | | | | | | | | | |
| t_{CD} | | Output | Chip Disable | | 20 | 35 | | 20 | 30 | ns |

NOTES:

1. Typical values are at $V_{\text{CC}} = 5\text{V}$, $T_{\text{amb}} = +25^\circ\text{C}$.
2. Tested at an address cycle time of $1\mu\text{s}$.
3. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS

